Claims

1. A soft metal conductor for use in a semiconductor device comprising grains having grain sizes sufficiently large so as to provide a substantially scratch-free surface upon polishing in a subsequent chemical mechanical polishing step.

2. A soft metal conductor having improved hardness in its uppermost layer for use in a semiconductor device wherein said uppermost layer consists of grains having grain sizes not smaller than about 20% of the thickness of said soft metal conductor.

3. A soft metal conductor according to claim 2, wherein said conductor is a member selected from the group consisting of a via, an interconnect and a line.

4. A soft metal conductor according to claim 2, wherein said soft metal is selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

5. An electrically conducting soft metal structure for use in a semiconductor device comprising:

an uppermost layer consisting of grains having grain sizes not smaller than about 20% of the thickness of said soft metal structure, and

a second layer contiguous with and immediately adjacent to said uppermost layer consisting of grains having grain sizes not larger than about 20% of the thickness of said soft metal structure.

6. An electrically conducting soft metal structure according to claim 5, wherein said uppermost layer having a thickness sufficiently large to provide a substantially scratch-free and erosion-free surface upon polishing in a chemical mechanical polishing method.

7. An electrically conducting soft metal structure according to claim 5, wherein said structure being made of a metal selected from the group consisting of aluminum, copper, silver, ternary and binary alloys of aluminum, copper, silver and any other low resistance metal.

8. An electrically conducting soft metal structure according to claim 5, wherein said structure being a member selected from the group consisting of a via, an interconnect and a line.

9. A soft metal conductor according to claim 2, wherein said uppermost layer consisting of grains of metal not less than 200 nm in grain size.

10. An electrically conducting soft metal structure according to claim 5, wherein said uppermost layer having grains of metal not less than 200 nm in grain size and a thickness of at least 100 nm.

11. An electrically conducting soft metal structure according to claim 5, wherein said uppermost layer having grains of metal not less than 200 nm in grain size and said second layer having grains of metal not more than 100 nm in grain size.

12. An electrically conducting soft metal structure according to claim 5, wherein said second layer having grains of metal not more than 100 nm in grain size and a thickness of not less than 600 nm.

13. An electrically conducting soft metal structure according to claim 5 further comprising a bottom layer contiguous with and immediately adjacent to said second layer, said bottom layer consisting of grain of metal not less than 200 nm in grain size.

14. A soft metal conductor for use in a semiconductor device comprising:

a first metal layer;

a Ti layer of less than 30 nm thick on top of said first soft metal layer,

a second metal layer on top of said Ti layer having in its uppermost surface metal grains of grain sizes not smaller than about 20% of the thickness of said second soft metal layer, and

whereby said Ti layer sandwiched between two soft metal layers is converted to $TiAl_3$ upon annealing at a temperature higher than room temperature such that diffusion of atoms of said soft metal through said Ti Al_3 film occurs upon the passage of an electrical current therethrough and thus improving the electromigration resistance of said soft metal conductor.

15. A soft metal conductor according to claim 14, wherein said soft metal is a member selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

16. A soft metal conductor according to claim 14, wherein said Ti layer further comprising composite layers of Ti and Ti alloys including Ti/TiN.

17. A soft metal conductor according to claim 14, wherein said Ti layer is situated at the bottom of a via having portions of said layer in extremely small thickness or portions of said layer in voids so as to allow the existence of a continuous phase of said soft metal material or diffusion of said soft metal atoms across a $TiAl_3$ layer subsequently formed and a resulting improvement in the electromigration resistance of said soft metal conductor.

18. A soft metal conductor according to claim 14 further comprising an annealing step at a predetermined temperature and for a predetermined length of time sufficient to convert said Ti layer to $TiAl_3$ when said soft metal used is Al or AlCu.

19. A soft metal conductor according to claim 18, wherein said predetermined temperature is not less than 300°C and said predetermined length of time is not less than 10 min.

20. A soft metal conductor according to claim 18, wherein said predetermined temperature is 400°C and said predetermined length of time is 30 min.

21. A method of making a soft metal conductor for use in a semiconductor device comprising the step of depositing a first layer of said soft metal consisting of grains having grain sizes sufficiently large such that a substantially scratch-free surface upon polishing in a subsequently conducted chemical mechanical polishing step is obtained.

22. A method according to claim 21, wherein said first soft metal layer is deposited by a technique selected from the group consisting of physical vapor deposition, chemical vapor deposition, evaporation and collimation.

23. A method according to claim 21, wherein said first soft metal layer consisting of grains of metal not less than 0.3 μm in grain size.

24. A method according to claim 21, wherein said first soft metal layer having a thickness of at least 100 nm.

25. A method according to claim 21 further comprising the step of depositing a layer of said soft metal consisting of grains having a grain size of not more than 200 nm and a layer thickness of not less than 400 nm prior to said deposition process of said first layer of soft metal having grains sufficiently large so as to provide a substantially scratch-free surface upon polishing in a subsequent CMP step.

26. A method according to claim 21 further comprising the steps of sequentially

depositing a layer of Ti of less than 30 nm thick and a second layer of soft metal on top of said first soft metal layer such that the anti-electromigration property of said soft metal conductor is improved when said Ti layer is converted to a $TiAl_3$ layer in a subsequent annealing process.

27. A method according to claim 21, wherein said soft metal is selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

28. A method of making a soft metal conductor in a semiconductor device comprising the steps of:

filling a cavity for conductor with a soft metal at a first temperature between about 100°C and about 300°C, said soft metal consisting of metal grains having a first grain size, and

heating said conductor to a second temperature and for a length of time sufficient to grow said metal grains to a second grain size larger than said first grain size.

29. A method according to claim 28, wherein said conductor is a member selected from the group consisting of a via, an interconnect and a line.

30. A method according to claim 28, wherein said soft metal is selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

31. A method according to claim 28, wherein said second temperature is not less than 300°C and said length of time is 2 min.

32. A method according to claim 28, wherein said second grain size is larger than said first grain size such that the polishing characteristics of said soft metal conductor is improved.

33. A method according to claim 28, wherein said second grain size is not smaller than 200 nm.

34. A method according to claim 28, wherein said first grain size is not larger than 200 nm and said second grain size is not smaller than 200 nm.

35. A method of polishing a soft metal structure according to a predetermined polishing process defined by the equation of:

$$\frac{dV}{dt} = \frac{KAR_{pd}H_pV_cG_p}{H_mG_m}$$

wherein dV/dt is the rate the volume of metal is removed, Hm is the hardness of the metal, H_p is the hardness of the particles in the slurry, A is the area of metal exposed, Gm is the grain size of metal, G_p is the grain size of the particles in the slurry, R_{pd} is the roughness of the polishing pad, K is a constant that depends on the chemical bonds between particles, metal,

pad, and pH factor, and V_c is the speed of the chuck, whereby said method allows an optimum volume of metal to be removed without scratching or R_{pd} erosion occurring in the metal.

36. A method according to claim 35, wherein the soft metal structure is a member selected from the group consisting of a via, an interconnect and a line.

37. A method according to claim 35, wherein said soft metal is selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

38. A method according to claim 35, wherein G_m is not smaller than 200 nm.

39. A dual-step deposition method for making a soft metal conductor for use in an electronic device comprising the steps of:

depositing a first layer of metal by a physical vapor deposition process to a first thickness, and

depositing a second layer of metal on top of said first layer of metal to a second thickness larger than said first thickness by a method selected from the group consisting of chemical vapor deposition, electroplating and electroless plating.

40. A dual-step deposition method for making a soft metal conductor according to claim 39, wherein said first and said second metal layer are deposited of a material selected from the group consisting of Al, Cu, Ag, CuAl, CuAg, AgAl and CuAgAl.

41. A dual-step deposition method for making a soft metal conductor according to claim 39, wherein said second metal layer deposited has an average grain size of not smaller than $0.1 \mu m$.

42. A dual-step deposition method for making a soft metal conductor according to claim 39, wherein said first thickness of said first layer of metal is at least 100 nm and said second thickness of said second layer of metal is at least 600 nm.

43. A dual-step deposition method for making a soft metal conductor according to claim 39, wherein the second layer of metal is deposited by a chemical vapor deposition technique at a reaction temperature of not less than 300°C.

44. A dual-step deposition method for making a soft metal conductor according to claim 39, wherein the first layer of metal deposited by a physical vapor deposition process comprises large grain Cu alloyed with an element selected from C, B, N or an element from the Periodic Table Group IIIA, IVA, VA for improved wear and electromigration resistance.

45. A dual-step deposition method for making a soft metal conductor according to claim 39, wherein said second layer of metal deposited has a sheet resistance of not higher than 0 1 Ω/□.

46. A dual-step deposition method for making a soft metal conductor for use in an electronic device comprising the steps of:

depositing a first layer of metal by a chemical vapor deposition technique to a first thickness, and

depositing a second layer of metal by a technique selected from the group consisting of electroplating, electroless plating and high temperature physical vapor deposition process.

47. A dual-step deposition method for making a soft metal conductor according to claim 46, wherein said first metal layer deposited has an average grain size of not smaller than 0.3μm.

48. A dual-step deposition method for making a soft metal conductor according to claim 46, wherein said first layer of metal deposited by a chemical vapor deposition technique has a sheet resistance of not higher than 0.1 Ω/□.

49. A method for forming an interconnect in a logic or memory device by at least two levels of metals comprising the steps of:

depositing at least one layer of metal into a line or via hole of a material selected from the group consisting of Cu, Ag, Al, CuAg, CuAl, AgAl and CuAgAl, and

depositing a final layer of Cu having an average grain size of not smaller than 0.3 μm on top of said at least one layer of metal into said line or via hole.

50. A method for forming an interconnect in a logic or memory device according to claim 49, wherein said at least one layer of metal comprising two layers of metal deposited into a line or via hole.

51. A method for forming an interconnect in a logic or memory device according to claim 49, wherein said final layer of Cu has a sheet resistance of not higher than 0.1 Ω/□.

52. A method for forming an interconnect surrounded at lest on three sides by an amorphous barrier layer comprising the steps of:

depositing an amorphous barrier layer of refractory metal nitride or carbide into a line or via hole by a vapor deposition technique, and

depositing a layer of a conductive metal having an average grain size of not smaller than 0.3 μm on top of said amorphous barrier layer filling said line or via hole.

53. A method for forming an interconnect encapsulated in an amorphous barrier layer according to claim 52, wherein said refractory metal in said refractory metal nitride or carbide is selected from the group consisting of W, Ta and Ti.

54. A method for forming an interconnect encapsulated in an amorphous barrier layer according to claim 52, wherein said conductive metal is selected from the group consisting of Cu, Ag, Al, CuAg, CuAl, AgAl and CuAgAl.

55. A method for forming an interconnect encapsulated in an amorphous barrier layer according to claim 52, wherein said vapor deposition technique is a chemical vapor deposition or a physical vapor deposition technique.

56. A method for forming an interconnect encapsulated in an amorphous barrier layer according to claim 52, wherein said refractory metal nitride is deposited by a chemical vapor deposition technique conducted at a reaction temperature between about 300°C and about 400°C.

57. A method for forming an interconnect surrounded in an amorphous barrier layer according to claim 52, wherein said refractory metal nitride is deposited by a sputtering technique by using a composite target.

58. A method for forming an interconnect encapsulated in an amorphous barrier layer according to claim 52 further comprising the step of annealing said amorphous barrier layer at a temperature of not lower than 400°C for at least ½ hour prior to the conductive metal deposition step.

59. A method for forming an interconnect encapsulated in an amorphous barrier layer according to claim 52 further comprising the step of depositing a seed layer of said conductive layer prior to the conductive metal deposition step.

60. A method for forming an interconnect surrounded at least on three sides by an amorphous barrier layer according to claim 52 further comprising the step of depositing a hard dielectric layer between said amorphous barrier layer and said conductive metal.

61. An electronic structure formed by the method of claim 59.

62. A method for forming a large grain interconnect encapsulated in an amorphous barrier layer according to claim 59, wherein said hard dielectric layer is deposited of a material selected from the group consisting of fluorinated oxide and amorphous or porous oxide treated with SiH_4 or CH_4.

63. A method for fabricating a single damascene structure having an interconnect formed of a metal selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl, said metal having substantially number of grains of a size larger than 0.3 μm

64. A method for fabricating a dual damascene structure having an interconnect formed of a metal selected from the group consisting of Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl, said metal having substantially number of grains of a size larger than 0.3 μm.

65. A method for forming an interconnect in an on-chip logic and memory (SRAM or DRAM) device by at least two levels of metals comprising the step of:

depositing at least one layer of metal into a line or via hole of a material selected from the group consisting of Cu, Ag, Al, and alloys of these elements, with average grain size of not smaller than 0.3 μm.

66. A semiconductor structure comprising logic and memory (SRAM or DRAM) devices interconnected through at least a via and one metal level,

the metal level and via comprising copper with grains of not smaller than 0.3 μm.